Power-Efficient Impedance-Modulation Wireless Data Links for Biomedical Implants

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Abstract—We analyze the performance of wireless data telemetry links for implanted biomedical systems. An experimental realization of a bidirectional half-duplex link that uses near-field inductive coupling between the implanted system and an external transceiver is described. Our system minimizes power consumption in the implanted system by using impedance modulation to transmit high-bandwidth information in the uplink direction, i.e., from the implanted to the external system. We measured a data rate of 2.8 Mbps at a bit error rate (BER) of $<10^{-6}$ (we could not measure error rates below $10^{-6}$) and a data rate of 4.0 Mbps at a BER of $10^{-7}$. Experimental results also demonstrate data transfer rates up to 300 kbps in the opposite, i.e., downlink direction. We also perform a theoretical analysis of the bit error rate performance. An important effect regarding the asymmetry of rising and falling edges that is inherent to impedance modulation is predicted by theory and confirmed by experiment. The link dissipates 2.5 mW in the external system and only 100 µW in the implanted system, making it among the most power-efficient inductive data links reported. Our link is compatible with FCC regulations on radiated emissions.

Index Terms—Impedance modulation, implants, load modulation, low power, near-field, telemetry, wireless.

I. INTRODUCTION

INDUCTIVELY COUPLED near-field wireless links have been extensively used in various implanted medical devices [1]–[7]. Some far-field links have also been reported [8]. Many of these links have been used to transmit power to the implanted device in addition to carrying unidirectional or bidirectional data signals. The system described in this paper was designed for use in an implanted neural prosthesis with multiple recording electrodes [9]. The prosthesis requires a wireless transcutaneous link to transmit data between the implanted subsystem and an external unit (see Fig. 1).

It is generally advantageous to separate the power and data transfer functions of a wireless link [10]–[12]. Power signals carry no information, and power transfer efficiency is maximized for narrowband (high-Q) links that operate at low frequencies to minimize losses in body tissue. On the other hand, data signals carry information and therefore require larger link bandwidths, which are more easily obtained at higher operating frequencies. Separating the two functions therefore allows them to be independently optimized, improving overall performance. In this paper, we therefore assume an independent power link is already present, and focus only on the data link. A detailed discussion of RF power link design may be found in [13].

Wireless power transfer may or may not be continuous. Continuous transfer uses an implanted rectifier, and may be avoided by incorporating a sealed rechargeable battery into the implant. In either case, the power dissipated by the implanted system should be minimized. Excess heat dissipated within the body results in tissue damage. In addition, the number of useful battery recharges is limited (typically to about $10^3$), so reducing implant power also prolongs battery life.

In implanted systems with many neural recording electrodes [14], the data rate from the implanted system to an external unit can be quite high since each electrode typically requires at least 5 kHz of bandwidth. We term this the uplink. Sending high-bandwidth data on the uplink is expensive in power. In this paper, we describe a wireless data link that solves this problem by pushing as much of the power and complexity to the external unit as possible. The power consumption of the external unit is less critical since its batteries may be easily changed. We also need a low-bandwidth data link from the external unit to the implanted unit for control, programming and feedback information. We term this data link the downlink. Our system minimizes implanted power in the downlink as well.

A brief version of this paper with preliminary results and no analysis was presented at a conference [15]. The current paper is organized as follows. A theoretical analysis of impedance modulation is carried out in Section II. The external and internal transceiver chips are described in Sections III and IV, respectively. The performance of the communication system is analyzed in Section V, while experimental results are presented in Section VI. Finally, Section VII concludes our discussion.

II. THEORETICAL ANALYSIS OF IMPEDANCE MODULATION

Our data link is designed to be half-duplex, i.e., either uplink or downlink data (but not both) can be transmitted at any given time. We use impedance modulation to transmit uplink data, while downlink data is transmitted via inductive coupling...
(transformer action). Impedance modulation, also known as load modulation, absorption modulation or backscattering, is a well-known technique used in RFID tags, low-power wireless sensors and biomedical implants [21–27]. One side (the source) of a coupled pair of resonators is driven with a sinusoidal source. The impedance of the other, load resonator is switched between two or more discrete states to transmit data. The resultant amplitude and/or phase modulation of the source waveform is detected to receive the data. The coupling between the resonators can be near-field (inductive) or far-field (radiative) in nature. In this section we theoretically analyze the performance of such communication systems. Our analysis simplifies and generalizes previous work, for example that in [21], [26], [27].

A. General Considerations

Assume a voltage source $v_G$ with an output impedance $Z_G$ is coupled to a load $Z_L$ via a linear, reciprocal two-port network. The situation is shown in Fig. 2, where $Z_{11}$ and $Z_{22}$ are the input impedances at the source and load terminals, respectively, with the other side open-circuited. In addition $Z_{12}$ is known as the transfer impedance between the source and load. It can be shown that the input impedances seen at the source and load terminals, denoted by $Z_T$ and $Z_R$, are given by

$$Z_T = Z_{11} - \frac{Z_{12}^2}{Z_{22} + Z_L}$$

$$Z_R = Z_{22} - \frac{Z_{12}^2}{Z_{11} + Z_G}$$

(1)

where the second term on the right-hand-side of each equation is known as the reflected impedance and is the net effect of the coupling network [13]. Equation (1) reveals that the transfer impedance of the coupling network acts as an impedance inverter (gyrator). The circuit shown in Fig. 2 is generic and can represent both near-field (reactive) and far-field (radiative) coupling between the source and load. For near-field coupling between two inductors $L_1$ and $L_2$, we have

$$Z_{11} = \omega L_1 + R_1$$

$$Z_{12} = \omega M$$

$$Z_{22} = \omega L_2 + R_2$$

(2)

Here $M$ is the mutual inductance between $L_1$ and $L_2$, while $R_1$ and $R_2$ are their series resistances. Notice that $Z_{12}$ is purely imaginary since the coupling was assumed to be purely reactive, with no energy lost due to radiation. In general the medium separating the coils has finite impedance $Z_m = R_m + j \omega C_m$, which will modify $Z_{11}$, $Z_{12}$ and $Z_{22}$ to new values $Z'_{11}$, $Z'_{12}$ and $Z'_{22}$. If the medium, such as biological tissue, has nonzero conductivity, i.e., $R_m \neq 0$, $Z'_{12}$ will contain a real component even in the absence of radiation. In addition, the reactance of the medium, $X_m$, will introduce capacitive coupling between the resonators. We shall ignore the effects of $Z_m$ to simplify our analysis. These assumptions are a good approximation for transcutaneous links unless the coils are designed to have very high values of $Q$ or the operating frequency is higher than $30–40$ MHz.

B. Impedance Modulation

Consider a near-field inductive link. The canonical example of this system is shown in Fig. 3(a), along with an equivalent representation in Fig. 3(b). For simplicity, we have ignored the impedance of the medium separating the coils. Consider this system in sinusoidal steady state. The source network is driven by a sinusoidal current source $i_G = I_{in} \sin(\omega t')$. However, Fig. 3(b) is identical to Fig. 2 if we use the relationships in (2) and also identify $Z_G = 1/(sC_1)$ and $Z_L = 1/(sC_2)$. We can therefore immediately use (1) to write

$$Z_{in} = \frac{v_1}{i_{in}} = Z_G + Z_T = Z_G + Z_{11} - \frac{Z_{12}^2}{Z_{22} + Z_L}$$

$$= \frac{1}{\omega^2 C_1} \frac{1}{\omega L_1 + R_1} + \frac{1}{\omega^2 M^2} \frac{1}{\omega L_2 + R_2}$$

$$= \frac{1}{\omega^2 M^2} \left( \frac{1}{\omega L_2 + R_2} + \frac{1}{\omega C_2} \right)$$

(4)

The system is usually operated around a frequency $\omega_0$ where both the source and load networks resonate, i.e., $\omega_0 = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_2 C_2}$. Let us define $Q_1 = \sqrt{L_1/C_1}/R_1$ and $Q_2 = \sqrt{L_2/C_2}/R_2$ to be the quality factors of the source and load networks, respectively. At the resonance frequency $\omega_0$, we can simplify (4) to

$$Z_{in} = R_1(1 + k^2 Q_1 Q_2) \equiv R_1(1 + m)$$

(5)

where the coupling coefficient between the inductors is denoted by $k$, defined as $k = M/\sqrt{L_1 L_2}$ where $0 < k < 1$, and is a function of coil geometry and separation. In addition, $m = k^2 Q_1 Q_2$ is known as the modulation index. In impedance modulation, the data to be transmitted changes the quality factor $Q_2$ of the load network, thereby modulating the voltage across the source network via the change in reflected impedance. The amount of modulation is maximized by making $Q_2$ zero in one
state, say when a ‘1’ is to be transmitted and $\gg 1$ in the other state (when a ‘0’ is transmitted). The latter scheme may be carried out by closing a switch to short-circuit the load network whenever a ‘1’ bit is to be transmitted, and opening the switch whenever a ‘0’ bit is to be transmitted. The resultant values of $v_1$ are then given by

$$v_1|_{\text{BIT}=0} = \frac{i_{\text{in}}}{R_1}$$

$$v_1|_{\text{BIT}=1} = \frac{i_{\text{in}}}{R_1(1+m)}$$

We see that impedance modulation causes amplitude shift-keying (ASK) of the source voltage $v_1$. Since $Z_{\text{in}}$ remains purely real in either state, phase modulation is absent. For simplicity, we shall assume that data bits are encoded as rectangular pulses.

The coupling coefficient $k$ typically decreases as $d^{-3}$, where $d$ is the separation between the coils. The strong dependence of $m$ on $k$ therefore makes impedance modulation unsuitable for long-range links. For short-range links, however, it possesses the great advantage of dissipating almost no power on the transmitting (load) side of the link. This advantage allows an implanted system to transmit data while keeping its power consumption to a minimum; most of the power is dissipated by the external unit.

C. An Alternative Topology

A practical problem with low-power implementations of the system shown in Fig. 3 is that $Z_{\text{in}}$ is on the order of $R_1$, which is usually just the series loss in the inductor $L_1$, and is quite small (on the order of a few $\Omega$). With any reasonable level of input current $i_{\text{in}}$, the result is extremely small voltage amplitudes $v_1$ across the network. This low impedance level may not be a problem when the inductive link is used to transfer power, but it is undesirable for data links. A simple way to increase the impedance across which $v_1$ is expressed is to convert the series resonant circuit shown in Fig. 3 into a parallel one, as shown in Fig. 4. The input current source $i_{\text{in}}$ is created by driving the gate of a transistor (which has transconductance $g_m$) with a sinusoidal voltage $v_{\text{in}}\sin(\omega t)$. Again, assuming that $\omega t = 1/\sqrt{L_1C_1} = 1/\sqrt{L_2C_2}$, we find that

$$Z_{\text{in}} = \frac{v_1}{i_{\text{in}}} \approx R_1(1+m) \left(\frac{Q_1}{1+m}\right)^2 = \frac{R_1 Q_1^2}{1+m}$$

with the approximation being valid if $k^2 Q_1 Q_2 + 1 \ll Q_1$, and we have used a series-to-parallel impedance transformation to derive the result. Since $Q_1 \gg 1$, this condition reduces to $k \ll 1/\sqrt{Q_2}$. It is instructive to rewrite (7) as follows:

$$Z_{\text{in}} = \frac{(R_1 Q_1)^2}{R_1(1+m)} = \frac{Z_0^2}{R_1(1+m)}.$$  

Here $Z_0 = R_1 Q_1 = \sqrt{L_1/C_1}$ and $k = k^2 Q_1 Q_2$, as before. We see that going from a series to a parallel resonant circuit has resulted in an impedance inversion (gyration) of the form $Z_{\text{in}} \rightarrow Z_0^2/Z_{\text{in}}$. The effective modulation depth $m_{\text{eff}}$ is now given by

$$m_{\text{eff}} = \left(1 - \frac{1}{1+m}\right) = \frac{m}{1+m}$$

and is approximately equal to $m$ if $m \ll 1$. The external resonator voltage amplitude switches between $v_1$ and $v_1/(1+m)$ based on whether a “1” or “0,” respectively, is being transmitted from the implanted unit. Equivalently, coupling to the internal resonator lowers the external resonator’s quality factor from $Q_1$ to $Q_1/\sqrt{1+m}$.

D. Downlink

During the downlink phase, the switch across the internal resonator is kept open. The amplitude of the RF voltage across the external resonator is modulated by the data; some of this amplitude variation is coupled to the internal resonator via the mutual inductance between $L_1$ and $L_2$. The voltage transfer function between the external resonator voltage $v_1$ and the internal resonator voltage $v_2$ is given by

$$m_d \equiv \frac{v_2}{v_1} = kQ_2\sqrt{\frac{L_2}{L_1}}.$$  

If we assume that the two coils are matched, so that $L_1 = L_2$ and $Q_1 = Q_2$, we see that $m_d = \sqrt{m}$. The amplitude of the received data signal is given by $m_d v_1$ for the downlink and $m_{\text{eff}} v_1$ for the uplink. The weaker dependence of $m_d$ on $k$ means that it falls off less rapidly with distance than $m$.

III. EXTERNAL TRANSCIEVER IMPLEMENTATION

We now describe the circuits used in our wireless data link. Separate internal and external transceiver chips have been designed and built. In this section we describe the transceiver designed for the external unit.

A. Front-End Circuits

A simplified schematic of the external transceiver is shown in Fig. 5. All analog circuits on the chip are biased using an on-chip 2 $\mu$A supply independent CMOS current reference. The current reference is cascaded to improve its output impedance; it also
uses a startup circuit that operates off the power supply turn-on transient and consumes no static power [28]. A power-on-reset circuit is used to ensure that all digital registers and latches initialize to a known state when the power supply is first turned on. The power-on-reset consists of a \( C - R \) circuit that differentiates the power supply turn-on ramp to produce a spike. This spike is converted to a logic-level global reset pulse by a Schmitt trigger.

The source resonator is incorporated into an RF oscillator, described later and shown in Fig. 8, that runs continuously when the transceiver is receiving data (\( TX \) is low). This arrangement saves power by combining the functions of the local oscillator and power amplifier into a single circuit. The internal transceiver uses a switch to short out or open-circuit its resonator (the load), thus modulating the envelope of the RF oscillator. Two envelope detectors, each using an MOS diode as the nonlinear element, individually track the positive and negative sides of the RF envelope (which move differentially). Each envelope detector (ED) leak current \( I_{\text{ED}} \) and load capacitor \( C_{\text{ED}} \) is set to 2 \( \mu \)A and 2.6 pF, respectively. These values are chosen so that the ED time constant \( \tau_{\text{ED}} \) is slow enough to filter out most of the RF carrier but fast enough not to significantly attenuate the data signal. The ED time constant is given by

\[
\tau_{\text{ED}} = \frac{C_{\text{ED}}}{g_{m,\text{diode}}} = \frac{C_{\text{ED}}/\phi}{I_{\text{ED}}}
\]  

The difference between the two ED outputs is amplified by an AC-coupled differential amplifier and fed into a comparator. The op-amps in this preamplifier are standard two-stage CMOS designs that consume 45 \( \mu \)A each. The values of the resistors \( R_1 \) and \( R_2 \) are 20 k\( \Omega \) and 100 k\( \Omega \), respectively; this choice makes the nominal gain of the preamplifier equal to \( G_A = 1 + R_2/R_1 = 6 \). The AC-coupling network uses \( C_3 = 10 \) pF and \( R_3 = 1 \) M\( \Omega \). We want to make the \( R_3C_3 \) time constant as large as possible to avoid signal attenuation during long runs of ‘0’ s or ‘1’ s, especially when the data rate is low. We use an asynchronous comparator that consists of a wide-output-swing operational transconductance amplifier (OTA) biased at a total current of 37.5 \( \mu \)A. The output current when the comparator is slewing is 30 \( \mu \)A.

Fig. 6 shows experimentally measured comparator inputs and output at a data rate of 2 Mbps. Feeding the two amplified envelopes differentially into the comparator increases our received signal-to-noise power ratio by a factor of 2 (3 dB) compared to a single-ended scheme that tracks only one side of the modulated RF signal.

The output of the comparator is passed into a hold timer circuit, shown in Fig. 7. The hold timer eliminates pulses that are shorter than a certain fixed duration. This strategy eliminates multiple transitions along data edges because of noise. The dead zones on the low-high and high-low input transitions are denoted by \( t_{\text{HL}} \) and \( t_{\text{LH}} \), respectively, and are given by

\[
t_{\text{HL}} = \frac{C_L(V_{\text{DDH}} - V_{\text{TL}})}{I_N}
\]
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\[ t_{HL} = \frac{C_L V_T H}{I_P} \]  \hspace{1cm} (12)

where \( V_{TH} \) and \( V_{TL} \) are, respectively, the low and high trip-points of the Schmitt trigger. The overall effect of the hold timer is similar to using a hysteretic comparator. The hold time for both low and high transitions was set to 100 ns. Its output is fed into a phase-locked loop (PLL) for clock and data recovery (CDR).

B. The RF Oscillator

Fig. 8 shows the RF oscillator. All components except \( L_1 \) are on-chip. The oscillator uses the resonant tank formed by \( L_1 \) and \( C_1 \) as the main frequency-selective element. A CMOS inverter in its high-gain region is used to provide enough loop gain to induce oscillations. Operation in this region is ensured by setting \( V_{DDL} \approx V_{DDH}/2 \), where \( V_{DDH} \) is the power supply for the inverter and the rest of the chip. The voltages \( V_{DDL} \) and \( V_{DDH} \) can be created by connecting two identical batteries in series.

The amplitude of the oscillation, \( V_1 \) (and power consumption) increases with the aspect ratio of the transistor in parallel with \( L_1 \) and \( C_1 \). The high-pass filter formed by \( R_2 \) and \( C_2 \) acts as a negative delay element (predictor) that cancels out the inverter delay \( t_{inv} \) [29].

If the inverter delay has been completely canceled, the oscillation frequency is simply given by \( \omega_0 = 1/\sqrt{L_1 C_1} \). By using an identical \( L_1 \) and \( C_1 \) as the internal resonator, we can now guarantee operation at the resonant frequency of both resonators. Since inductor and capacitor values match well, the need for any additional frequency-tuning is eliminated. It can be shown that, in order for the inverter delay to be completely canceled, we must have

\[ R_2 C_2 = \frac{1}{\omega_0 \tan(\omega f_{inv})}. \]  \hspace{1cm} (13)

Increasing the oscillation frequency \( f_{osc} \) increases the quality factors of the inductors, which increases \( m_{Qf} \), allowing smaller oscillation amplitudes to be used and thereby lowering power consumption. However, at very high frequencies the coils eventually self-resonate and losses due to body tissues also increase, effectively lowering \( Q \). In our case a good compromise between these competing factors was obtained around 25 MHz, which is where we operate.

C. The Phase-Locked Loop

The PLL, shown in Fig. 9, allows the uplink to use nonreturn (NR) data encoding, which maximizes data rate for a given link bandwidth. It uses a Hogge-type phase detector (PD) [30], shown in Fig. 10, a cascoded charge pump and a passive, third-order loop filter. The charge pump uses differential switching to reduce charge injection errors (see Fig. 11). The loop filter contains two additional high-frequency poles (indicated in the figure) that are placed beyond the crossover frequency of the loop transmission. These poles filter out high-frequency ripple on \( V_{OUT} \), thereby reducing jitter in the output clock while only minimally degrading the phase margin of the loop. The reference voltage \( V_{REF} \) is normally set to \( V_{DDL} \), which is a convenient value midway between the rails.
The output of the loop filter, $V_{OUT}$, is converted to a current by a wide-linear-range transconductor (WLR) [31] that combines a well-input differential pair and other linearization techniques to achieve over 1.5 V of input linear range. The output current of the WLR, $I_{WLR}$, is fed into a current-starved ring oscillator (CCO). The loop bandwidth is set to 20 KHz (about 1% of the nominal data rate, which is 2 Mbps). This value is low enough to ensure that the loop remains locked even when long “runs” of consecutive “1s” or “0s” occur in the input data stream. The loop locks when the CCO frequency is twice the data rate (a result of using the Hogge PD, which also outputs re-timed data with edges synchronized to the recovered clock).

True phase detectors, such as the Hogge, do not provide much frequency error information. This property enables a CDR PLL to remain locked when missing edges appear in the input data stream, but reduces its capture range. As a result, CDR PLL’s usually need additional circuitry to aid acquisition of lock. We have designed a frequency-locked loop (FLL) for this purpose. The FLL is shown in Fig. 12. A timer activates it for a fixed number of clock cycles after a system reset (see Fig. 9). During this period, the main PLL is disabled and the internal unit transmits a synchronization sequence consisting of alternating ‘0’ and ‘1’ bits. The FLL is a first-order loop that counts clock and data edges and sets the bias current of the CCO so that their rates are equal. It does this by using a digital accumulator (which acts as the loop filter) and current DAC. Each data edge (rising or falling) increments the accumulator, while the divide-by-2 circuit ensures that only rising clock edges decrement it. Therefore, the FLL, like the PLL itself, is locked when the clock runs at double the data rate. When the timer disables the FLL the CCO is already running close to the right frequency, so the PLL locks more easily. In our implementation, the accumulator and DAC have five bits each, which limits the initial frequency error that must be handled by the PLL to less than 1/2^5 ≈ 3% of the data rate.

Fig. 13 shows experimentally measured oscillator output (i.e., clock) frequencies as a function of the loop filter output voltage for two different power supply voltages. The loop filter output voltage is fed into the WLR transconductor to generate the CCO control current $I_{WLR}$. The measured curves are fairly linear, but the slope changes noticeably when $V_{DDH}$ is changed from 2.8 to 3.3 V, indicating that the tuning gain of the CCO changes with $V_{DDH}$. This change occurs because $t_{del}$, the delay of each current-starved inverter forming the CCO, increases with $V_{DDH}$. In fact, if the pMOS and nMOS sides are ratioed such that the inverters are balanced, the threshold voltage must be approximately $V_{DD}/2$. Therefore, to first order we have $t_{del} \approx C_{L}V_{DD}/(2I_{CCO})$.

D. Downlink

During the transmit phase ($TX$ is high in Fig. 5) data is sent to the implanted system via on-off keying (OOK). In this phase the data signal turns the oscillator on and off (see Fig. 8), thus changing the amplitude of the voltage across the source resonator from $v_1$ to 0. This change $v_1$ is coupled to the load resonator (in the implanted unit) by transformer action between $L_1$ and $L_2$. The amplitude of the voltage across it varies between $v_2$ to 0, where $v_2/v_1 = m_d$ and $m_d$ is given by (10). To save power, all receiver circuits in the external unit are turned off during this phase.

Downlink data is encoded using 25/75% pulsewidth modulation (PWM) before transmission using a counter-based on-chip modulator. Pulse-width modulation, pulse-position modulation and other return-to-zero (RZ) encoding schemes are spectrally
inefficient. However, it makes sense to use an RZ scheme for the downlink since the data rate is low in this direction. Every bit period in RZ data contains at least one level transition that can be used as a clock edge. Therefore, a PLL is not needed for CDR in the implanted system, minimizing its complexity and power consumption.

IV. INTERNAL TRANSCEIVER IMPLEMENTATION

A simplified block diagram of the internal transceiver is shown in Fig. 14. All analog circuits on the chip are biased using an on-chip 0.2-μA CMOS current reference. During the transmit phase (TX is high in Fig. 14), the data stream to be transmitted turns the impedance-modulation switch $M_2$ in parallel with the load resonator on and off. To save power, all receiver circuits in the internal unit are turned off during this phase.

During the receive phase (TX is low) the impedance-modulation switch is turned off and an envelope detector is used to track the voltage on the load resonator. This voltage follows the PWM-encoded OOK bitstream transmitted from the external transceiver. The output of the envelope detector is compared with a reference voltage $V_{\text{ref}}$ that is implicitly generated by making the MOS diode connected to the negative input terminal of the comparator 16 times wider than that connected to the positive terminal. Since the two diodes carry the same current, in the absence of any coupled signal the voltage on the negative terminal exceeds that on the positive terminal by $V_{\text{ref}} = (\phi_0/\kappa)\ln(16) \approx 96\, \text{mV}$, and the comparator output is low (here $\kappa \approx 0.75$ is the subthreshold constant). It goes high only when enough signal is coupled into $L_2$ for the voltage at the positive terminal to increase by an amount greater than $V_{\text{ref}}$.

The value of $V_{\text{ref}}$ is chosen to be large enough to comfortably exceed the unknown input-referred offset voltage of the comparator, which is usually in the range of 10–20 mV.

The envelope detector time constant is $\tau_{\text{ED}} = R_{\text{ED}}C_{\text{ED}}$, where $R_{\text{ED}} = 500\, \text{k}\Omega$ and $C_{\text{ED}} = 5.2\, \text{pF}$. The comparator is a wide-output-swing OTA biased at a total current of 0.5 μA. A hold timer, similar to the one in the external transceiver, is used to remove spurious transitions in the comparator output waveform due to noise. The hold time for both low and high transitions was set to 1 μs. The diode $D_2$ is a parasitic p-n junction diode present between the source/drain and well terminals of $M_2$. It clamps the voltage across the internal resonator if its amplitude exceeds one diode drop (about 0.6 V).

The output of the hold timer, $V_{\text{PWM}}$, is fed into a pulsewidth demodulator circuit that regenerates the downlink data stream from the PWM waveform. The demodulation circuit, shown in Fig. 15, uses two capacitors, of value $C_A$ and $C_B$, and charges them using the currents $I_A$ and $I_B$ when the PWM waveform is high and low, respectively. At the end of a bit period, the voltages across the capacitors, $V_A$ and $V_B$, are compared to determine if the bit transmitted was a ‘0’ or a ‘1’. The capacitors are then reset and the process starts again for the next bit. The reset pulses $R_1$ and $R_2$ are obtained by digitally differentiating $V_{\text{PWM}}$.

A reasonable way to optimize the circuit is to require that $\Delta V_0 = -\Delta V_1$, where $V_0$ ($V_1$) is the difference between $V_A$ and $V_B$ at the end of a ‘0’ (‘1’) bit. Assuming that “0” and “1” bits are equally likely, this condition minimizes the bit error rate for a given signal-to-noise ratio. It can be shown that, in this optimal situation, we must have

$$\frac{(I_A/C_A)}{(I_B/C_B)} = \left(\frac{2}{\alpha_0 + \alpha_1} - 1\right)$$

(14)

where $0 < \alpha_0 < 1$ and $0 < \alpha_1 < 1$ are the pulse widths (normalized by the bit period) used to signal ‘0’ and ‘1’, respectively. In our case $\alpha_0 = 0.25$ (high pulse = 25% of bit period) and $\alpha_1 = 0.75$ (high pulse = 75% of bit period). From (14)
we should use \((I_A/C_A)/(I_B/C_B) = 1\). To simplify layout, we make \(I_A = I_B\) and \(C_A = C_B\).

V. PERFORMANCE ANALYSIS

In this section we theoretically analyze the performance of our communication system. This analysis will be important later for showing that the experimental performance of our system matches that predicted by theory.

A. Pulse Width Distortion Mechanism

The voltage across the implanted resonator has asymmetric rising and falling edges because its quality factor \(Q_2\) is different in the two states (switch OFF and ON, respectively). When the switch is turned off, the voltage gradually increases (with an exponential envelope) since \(Q_2\) is high. On the other hand, when the switch is turned on, the voltage quickly dies away since \(Q_2\) is now approximately zero (see Fig. 16).

The envelope of the external resonator voltage is a lowpass filtered version of that on the implanted resonator, since the external resonator behaves like a lowpass filter centered around the carrier frequency. The corner frequency of the lowpass filter formed by the external resonator is constant since its quality factor \(Q_1\) remains almost constant. To first order, filtering provided by the external resonator adds an equal amount of delay to rising and falling edges. As a result, the detected external envelope continues to have rising data edges that are delayed relative to the falling edges. Hence, \(0\rightarrow1\) transitions are delayed compared with \(1\rightarrow0\) transitions, as shown in Fig. 16. Therefore, the length of the first “1” bit in a continuous sequence of “1” bits is shortened. Fig. 6 illustrates that isolated “1” bits have a shorter pulsewidth compared to isolated “0” bits, another manifestation of this effect.

An additional complication, also illustrated in Fig. 16, is that diode clamping occurs when the peak internal voltage \(V_2\) exceeds 0.6 V. Under these conditions, the parasitic source/drain junction diode \(D_2\) associated with the switch \(M_2\) (see Fig. 14) turns on, clamping \(V_2\) and preventing it from increasing further. This effect only occurs when \(V_2 = m_d V_1\) exceeds \(V_D\), where \(m_d\) is the voltage transfer function between the internal and external resonator voltages [given by (10)], \(V_1\) is the amplitude of the external resonator voltage (set by the RF oscillator), and \(V_D \approx 0.6\) V is the turn-on voltage of diode \(D_2\), which we assume to be approximately constant. Although diode clamping in Fig. 14 occurs only when \(V_2\) is larger than \(V_D\) by \(V_D\), the bandpass nature of the \(L_2 C_2\) circuit transforms asymmetric clamping to symmetric clamping in \(V_2\). The inductor \(L_2\) and capacitor \(C_2\) in Fig. 14 together form a high-\(Q\) filter centered around the carrier frequency when the switch \(M_2\) is open, thus ensuring that the positive and negative envelopes of the voltage across the internal resonator are both equal to \(V_D\) (as shown in Fig. 16).

The comparator in the external transceiver compares the positive and negative envelopes of the RF oscillator. These envelopes are differential signals (see Fig. 5). Therefore, the comparator output switches state when the envelope voltages reach their average (DC) value. It is conceptually easy (but algebraically tedious; for details, please see the Appendix) to show that \(t_{\Delta t}\), the mean delay of rising data edges, is

\[
t_{\Delta t} = \tau_2 \ln(2) - \tau_1 \ln(2 - \alpha), \quad m_d V_1 < V_D
\]

\[
\approx \tau_2 \ln(2) - \tau_2 \ln \left(2 - \frac{\alpha V_D}{m_d V_1}\right), \quad m_d V_1 \geq V_D \tag{15}
\]

where \(\tau_1 = 2 Q_1 / \omega_1\) and \(\tau_2 = 2 Q_2 / \omega_2\) are the time constants of the external and internal resonator voltage envelopes, respectively. The parameter \(\alpha\) is the mean (DC) voltage of the envelope waveform normalized to its ideal value, which is half the peak voltage. Since we get high pulses that have less area than low pulses, \(\alpha < 1\). Equation (15) captures two physical effects. Firstly, diode clamping serves to “speed up” time constants because RF waveforms start to look more like square waves. Secondly, a nonsymmetric duty cycle in the envelope waveforms \((\alpha < 1)\) causes zero crossings to occur before the halfway point between the “low” and “high” levels is reached, again reducing delay.

The exact value of \(\alpha\) depends on statistical properties of the data stream that establish its mean (DC) value. We see from (15) that \(t_{\Delta t}\) remains constant with \(m_d\) when \(m_d\) is small, and then gradually decreases. Since \(m_d \propto k\), we expect \(t_{\Delta t}\) to remain constant with coil separation when the coils are far apart, and then gradually decrease, following (15), as they are brought together. We also found that comparator voltage offset, another potential source of pulsedwidth distortion, was not significant.

B. Bit Error Mechanism

Bit errors occur when the PLL samples the wrong value for the input bit. As long as both ‘0’ and ‘1’ data bits have the same length (i.e., there is no duty cycle distortion in the input) and the PLL is locked, rising clock edges are aligned with input data transitions. As a result, the Hogg phase detector samples the input data stream in the middle of each input bit. This fact may be seen from the circuit diagram shown in Fig. 10. When the recovered clock from the VCO goes low, the current value of the input data stream is sampled by the D-register \(R_1\). This value...
appears at the output of the D-latch $L_1$ (as the re-timed data bit) half a bit period later, when the clock goes high. It is easy to see that an error will occur if the rising data edge is delayed by more than half a bit period with respect to the negative edge of the clock, or the falling edge advanced by the same amount. In either case, the clock samples the wrong data value, i.e., “0,” rather than its correct value, i.e., “1.”

We call the mean value of the time between data transitions and negative clock edges the *time window* $t_w$. It is easy to see that, when no duty-cycle distortion is present, $t_w = T/2$, where $T$ is the bit period.

For simplicity, consider a PLL with no timing offset and 50% duty cycle in the recovered clock. In the presence of duty cycle distortion in the input data stream, rising clock edges can no longer remain aligned with both rising and falling data transitions since this would make the clock nonperiodic. The PLL resolves this situation as shown in Fig. 17: it shifts the phase of the clock such that there is equal but opposite timing error at both types of data transitions. In other words, the PLL ensures that the delay between rising clock and rising data edges is equal to that between falling data and rising clock edges. Since the two timing errors are equal, equal-width “UP” and “DN” signals are generated by the Hogg phase detector whenever a data transition occurs. As a result, the average charge being fed into the loop filter remains zero, i.e., the PLL remains locked.

Asymmetric rising and falling waveforms in the internal resonator cause duty-cycle distortion: rising data edges are delayed relative to falling edges by an amount equal to $t_{dr}$, thereby making “1” bits shorter than “0” bits. At lock, the PLL will divide any timing error equally between rising and falling data edges. Therefore, the timing error at each data transition becomes $t_{dr}/2$. Thus, errors at rising and falling transitions occur with equal probability: either the first or the last “1” in a run of several “1” bits can be sampled incorrectly, resulting in bit errors. The time window $t_w$ we have for sampling the data correctly is now given by

$$t_w = \frac{T}{2} - \frac{t_{dr}}{2}. \quad (16)$$

Both the input to the PLL and the clock contain random timing jitter. Jitter in the input data stream is caused by voltage noise that is present at the output of the comparator while it is changing state. Such noise is generated by the envelope detectors, the differential amplifiers and the comparator itself. Some of the jitter in the synthesized clock is caused by input jitter that has been lowpass filtered by the PLL, while the rest is introduced by the VCO. The presence of timing jitter makes $t_w$ a random variable (see Fig. 17); its variance is given by

$$\sigma_{tw}^2 = \sigma_{data}^2 + \sigma_{clk}^2 \quad (17)$$

where we have assumed that $\sigma_{data}$ and $\sigma_{clk}$, the timing jitters of the input data and synthesized clock, respectively, are uncorrelated with each other and equal for positive and negative transitions in both waveforms. Assuming Gaussian (normal) probability distributions for both these quantities, the probability that the PLL samples an incorrect value is given by

$$P_e = \frac{1}{2} \text{erfc} \left( \frac{t_w}{\sqrt{2\sigma_{tw}^2}} \right). \quad (18)$$

### C. BER Calculation

We used a maximal-length pseudo-noise (PN) sequence of length $2^N - 1$, generated on-chip by the internal transceiver, to test the uplink. Since most of the bit errors happen because of timing error at data transitions, the bit error rate (BER) of the system is dominated by errors where the *first or last* bit in a run (consecutive sequence) of ‘1’ bits is misread as a ‘0’. The BER is thus given by

$$\text{BER} = P_e \times \left( P_{1,1} + \sum_{n=2}^{N} 2P_{1,n} \right) \quad (19)$$

where $P_e$ is given by (18), $P_{1,n}$ is the probability that a run of $n$ “1s” occurs, and the longest runs are $N$ bits long. This equation expresses the fact that we can get two, and only two, bit errors whenever we have runs of two or more “1s.” For maximal-length PN sequences, it can be shown that $P_{1,n}$ decreases exponentially with $n$ [32], i.e.,

$$P_{1,n+1} = \frac{1}{2} P_{1,n}, \quad (N - 1) \geq n \geq 1. \quad (20)$$

Maximal-length PN sequences are almost balanced: the number of “1s” is only one more than the number of zeros. Therefore, the probability of a given bit being a “1” approaches 1/2 for large values of $N$, i.e., $\sum_{n=1}^{\infty} nP_{1,n} = 1/2$. We can solve this equation by using (20). The result is

$$P_{1,n} = \frac{1}{2^{n+1}}. \quad (21)$$

By substituting (21) into (19) and approximating the sum as an infinite series (i.e., assuming that $N \to \infty$), we find that

$$\text{BER} \approx 3P_e/8. \quad \text{Therefore, from (18), our overall BER is given by}$$

$$\text{BER} \approx \frac{3}{16} \text{erfc} \left( \frac{t_w}{\sqrt{2(\sigma_{data}^2 + \sigma_{clk}^2)}} \right). \quad (22)$$

Since the run-length statistics of PN sequences are known (see (21)), we can also calculate the value of $\alpha$, the normalized mean voltage of the external resonator envelope waveform.
Using (15), we can then analytically find the time delay $t_{\text{dr}}$. We find that, to a very good approximation

$$
\alpha = 1 - \frac{\tau_2}{T} \left( 1 - e^{-T/\tau_2} \right), \quad \beta < 1
$$

$$
= 1 - \frac{\tau_2}{2T} \left( 1 + (\beta - 1) \ln \left( 1 - \frac{1}{\beta} \right) \right), \quad \beta \geq 1 \quad (23)
$$

where the parameter $\beta = m_d V_i/V_D$. For a detailed derivation of this equation, please see the Appendix.

### D. Downlink

During the downlink, the voltage across the internal resonator is modulated by turning the external oscillator ON and OFF. The internal resonator is always in a high-$Q$ state. Therefore, to first order, rise and fall times are equal and no pulsewidth distortion occurs. In addition, the data rate is much lower for the downlink, reducing sensitivity to any residual duty cycle distortion mechanism. As a result, uplink limitations dominate the performance of our system. Therefore, we do not further analyze the downlink.

### VI. EXPERIMENTAL RESULTS

Separate external and internal transceiver chips, each 1.5 mm $\times$ 1.5 mm in size, were fabricated in the AMI 0.5-$\mu$m CMOS process. Fig. 18 shows die photographs of both chips. About 40% of the core area of the external transceiver chip (shown on the right) is occupied by the resistors and capacitors in the PLL loop filter. The internal transceiver chip is shown on the left.

Fig. 19 shows the two printed circuit boards that were used to test the wireless link. Identical transmit and receive coils were printed on the boards. Each coil was square, 3.5 cm on a side and had two turns. The designed inductance was 500 nH with a simulated quality factor of 30 at 25 MHz. Packaged chips were surface mounted on the boards and they were aligned parallel to each other at various separations for testing. No external components were needed apart from the coils, decoupling capacitors and power supplies.

Implanted coils are typically $<2$ cm on a side and operate at link distances between 0.3 and 1 cm. However, our coils are somewhat larger than average (3.5 cm on a side). To reduce the coupling constant $k$ to more typical values, and allow for possible coil misalignment, we tested our link over larger distances (between 1.5 and 5 cm). Fig. 20 shows the measured value of the effective modulation depth for the uplink as a function of $r$, the separation between the coils. We expect the coupling between the coils to vary approximately as $k \propto (a^2 + r^2)^{-3/2}$, where $a = 2$ cm is the radius of a circular coil with the same area as our square coils. We get a good fit to the measured data using this model for $k$ when we assume that the internal voltage is clamped to a maximum of $V_D = 0.6$ V. $Q_1 = 10$ and $Q_2 = 25$. The fit is relatively insensitive to the exact value of $Q$ and $V_D$. The value of $Q_1$ is significantly lower than the predicted quality factor of the unloaded coil (about 30) because of the finite output impedance of the transistor $M_1$ in Fig. 8. Fig. 20 also shows that ignoring the diode clamp predicts much higher values of modulation index than are actually observed.

Fig. 21 shows transmitted and received data and recovered clock waveforms measured for the uplink at 5.8 Mbps with the coils 2 cm apart. The PLL synchronizes rising edges of the recovered clock to data transitions. Falling edges of the clock therefore appear in the middle of each bit and are used to sample the data stream. At this separation, the PLL was observed to lock over data rates varying between 1 and 5.8 Mbps. The upper end of the lock range is set by the loop filter, which runs out of linear range and hits $V_{\text{DDH}}$. At low data rates the loop filter voltage becomes low enough to turn on the well-source diode present at
the input of the wide-linear-range transconductor [31], thus setting the lower end of the lock range. Notice that isolated “1” bits at the output of the comparator are significantly narrower than isolated “0” bits. This effect, which is also visible in Fig. 6, is a manifestation of the pulsewidth distortion mechanism discussed in the previous section.

The top plot in Fig. 22 shows typical experimentally measured transitions in the comparator output. Many transitions have been overlaid on top of each other to evaluate the statistics of the threshold-crossing instant. The probability distribution function (pdf) of this random variable is shown in the lower plot. We see that the pdf shows two distinct peaks. The first peak is produced by falling edges, while rising edges produce the second peak. The pdf is fit to a model consisting of a weighted sum of two Gaussian distributions. The results of the fit are also shown on the lower plot. The difference between the means of the two Gaussian distributions constitutes the amount of pulsewidth narrowing measured under these conditions. The standard deviations of the two Gaussian curves are approximately equal, confirming one of our earlier assumptions. This measured quantity is $\sigma_{\text{data}}$, the rms jitter of rising data edges.

The measurements shown in Fig. 22 were repeated for various data rates and link distances. Similar time-domain measurement techniques were used to also find $\sigma_{\text{clk}}$, the rms jitter of the clock produced by the PLL. The results were found to depend weakly on data rate but strongly on link distance. To reduce measurement errors, $\sigma_{\text{data}}$, $\sigma_{\text{clock}}$, and $\sigma_{\text{clk}}$ were therefore averaged over the data rate. The resultant values are plotted in Figs. 23(a) and 23(b) as a function of the link distance. The rms clock jitter $\sigma_{\text{clk}}$ remains almost constant with link distance. Its average value is 7.2 ns.

The measured delay was also fitted to the value predicted by theory, i.e., (15), with $\alpha$ given by (23). An excellent fit was obtained, as shown in Fig. 23(a).

Fig. 24 shows experimentally measured BER for the wireless uplink when the coils were placed 2, 3, and 4 cm apart. Error rates less than $10^{-6}$ could not be measured with our experimental setup in a reasonable amount of time. Experimentally measured values of $t_{\text{delay}}$, $\sigma_{\text{delay}}$, and $\sigma_{\text{clk}}$ were also plugged into
(22) to draw predicted BER curves. The experimentally measured BER values match well with those predicted theoretically for the 2 cm case. The predicted values are significantly lower than the experimental values for the two other link distances, implying the existence of an additional error mechanism. Experimental evidence indicates that transient loss of lock (so-called cycle-slipping) becomes increasingly common as the link distance increases and the received signal-to-noise ratio decreases. This process may account for the increased number of bit errors at large link distances. Our hypothesis is supported by the fact that the lock range of the PLL (which limits the range of data rates for which we could measure BER) decreases as the link distance increases.

Fig. 25 shows transmitted and received data waveforms (before and after pulsewidth demodulation) measured for the downlink at 200 kbps with the coils 2 cm apart. Recovered data transitions are aligned with rising edges of the pulsewidth modulated signal. Falling edges of this signal can therefore be used to sample the data stream. The downlink was observed to operate over data rates varying between 15 and 300 kbps. When the data rate is less than 15 kbps the capacitor voltages $V_A$ and $V_D$ in the PWM demodulator (see Fig. 15) hit $V_{DD}$ before the bit period $T$ is complete, resulting in demodulation errors. When the data rate is greater than 300 kbps the bit period becomes smaller than the minimum allowable pulsewidth in the data waveform (set to 1 $\mu$s by the hold timer). The hold timer starts ignoring data transitions separated by a single bit period, again resulting in errors.

We have also measured the BER for the downlink. No bit errors were observed when the coils were placed 2 cm apart and approximately 2x10^5 bits were transmitted at data rates varying between 15 and 300 kbps. Assuming bit errors follow Poisson arrival statistics, we can therefore say, with approximately 85% confidence, that the downlink BER is less than 10^{-5} over the tested range of data rates.

We tested two sets of chips and boards. No major differences in performance were noted between them. We also inserted a 2-cm-thick layer of 0.9% saline solution between the coils and repeated some of our tests. As in prior reports, for example [7], the goal was to verify that the wireless link would operate normally in the presence of body tissue. No significant differences in performance were noted. We have also estimated the amount of power radiated by our system (see Appendix). The calculation shows that our current design meets regulatory requirements in the United States for unlicensed, low-power wireless devices.

VII. CONCLUSION

We have presented a low-power bidirectional wireless link for biomedical implants and analyzed its performance. Table I summarizes the measured performance of our bidirectional wireless link. A useful figure of merit that characterizes the efficiency of any communication system is the energy consumed per bit $E_{bit}$, which is defined as

$$E_{bit} = \frac{P_{diss}}{R}$$

where $P_{diss}$ is the total power dissipation and $R = 1/T$ is the data rate. Significant power optimization can be carried out on our current design. For example, the RF oscillator’s power consumption can be considerably reduced by adapting its power supply voltage $V_{DD}$ based on the value of $k$. Nevertheless, we get $E_{bit} = 0.56$ nJ/bit for a bit error rate of $< 10^{-5}$ and 2 cm

TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link distance</td>
<td>tested up to 5 cm</td>
</tr>
<tr>
<td>Center frequency</td>
<td>25 MHz</td>
</tr>
<tr>
<td>Uplink data rate</td>
<td>1 Mbps - 5.8 Mbps (at 2 cm)</td>
</tr>
<tr>
<td>Uplink encoding</td>
<td>Non-return (NR)</td>
</tr>
<tr>
<td>Downlink data rate</td>
<td>15 kbps - 300 kbps (at 2 cm)</td>
</tr>
<tr>
<td>Downlink encoding</td>
<td>Pulse-width modulation (PWM)</td>
</tr>
<tr>
<td>Power supply voltages $V_{DD}/V_{DDL}$</td>
<td>2.8 V / 1.4 V</td>
</tr>
<tr>
<td>External power consumption</td>
<td>2.5mW (uplink) / 1.5mW (downlink)</td>
</tr>
<tr>
<td>Internal power consumption</td>
<td>100µW (uplink) / 140µW (downlink)</td>
</tr>
<tr>
<td>Fabrication process</td>
<td>AMI 0.5µm CMOS</td>
</tr>
<tr>
<td>Chip size</td>
<td>1.5mmx1.5mm (each transceiver)</td>
</tr>
</tbody>
</table>
coil separation. We were unable to measure bit error rates below $10^{-6}$ in reasonable amounts of time so this bit-error rate should only be viewed as an upper bound.

Table II compares our uplink to wireless data links for biomedical implants that have recently been reported in the literature. The link described in [8] is a far-field link, while the others are inductive near-field links. Ideally it should be possible to compare the efficiencies of these designs by using energy consumed per bit as the metric. However, in each case what is available is not the power consumed by the the entire communication system, but by the receiver or transmitter alone. The absence of total power consumption data makes quantitative system efficiency comparisons difficult. However, attractive features of our design include high data rate, low bit error rate and extremely low power consumption in the internal unit.

We conclude by discussing two techniques for further improving the performance of our wireless link. We have simulated these techniques and plan to implement them on a future design iteration.

### A. Resonator Amplitude Control

The RF amplitude across the external resonator can be reduced to save power when the modulation depth $m_{\text{off}}$ is high enough. There are three main parameters of the current design that can be varied to control this amplitude: the power supply voltage $V_{\text{DDL}}$, the aspect ratio of the transistor $M_2$ that drives the external resonator and, finally, the conduction angle $\theta$, i.e., the fraction of the oscillation period during which $M_2$ conducts current. Alternatively, a more easily controllable oscillator topology can be used. For example, in a Colpitts oscillator amplitude can be conveniently controlled using bias current.

### B. Soft Switch Turn-On

As discussed in this paper, the main cause of uplink bit errors is pulselwidth distortion caused by asymmetric rising and falling waveforms in the internal resonator. A simple technique that substantially reduces this effect is to turn on the switch $M_2$ (shown in Fig. 14) in a "soft," i.e., gradual way. By slowing down the falling edges of the resonator voltage waveform, this technique decreases $t_{\text{dr}}$, the amount of pulselwidth narrowing caused by the resonators. A basic circuit implementation of this idea uses an inverter that is current starved on the pull-down, i.e., nMOS side to drive $M_2$. The value of the maximum pull-down current is set using feed-forward or feedback to ensure equal delay on rising and falling edges.

---

**TABLE II**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Coil diameter (Tx/Rx)</th>
<th>Link distance</th>
<th>Carrier frequency</th>
<th>Data rate</th>
<th>BER</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>2cm/1.2cm</td>
<td>0.5cm</td>
<td>5MHz/10MHz</td>
<td>2.5Mbps</td>
<td>$10^{-6}$</td>
<td>0.38mW (Rx only)</td>
</tr>
<tr>
<td>[6]</td>
<td>3.5cm/2.7cm</td>
<td>1.5cm</td>
<td>10MHz</td>
<td>1.12Mbps</td>
<td>$10^{-5}$</td>
<td>0.61mW (Rx only)</td>
</tr>
<tr>
<td>[8]</td>
<td>0.47mm/35cm (antenna)</td>
<td>13cm</td>
<td>433MHz</td>
<td>330kbps</td>
<td>$3 \times 10^{-3}$</td>
<td>1.81mW (Tx only)</td>
</tr>
<tr>
<td>This work</td>
<td>3.5cm/3.5cm</td>
<td>2cm</td>
<td>25MHz</td>
<td>2.8Mbps</td>
<td>$&lt;10^{-6}$</td>
<td>0.1mW (Tx)/2.5mW (Rx)</td>
</tr>
</tbody>
</table>

---

**APPENDIX**

### A. Derivation of Equation (15)

Consider the envelope of the voltage on the secondary resonator. In the absence of diode clamping, i.e., $m_4 V_1 < V_D$ or $\beta < 1$, the voltage increases like an RC circuit with time constant $\tau_2$ from zero towards its peak value $m_4 V_1$. However, as shown in Fig. 26, it falls abruptly to zero. The delay $t_{\text{dr}}$ is equal to the length of time taken by the voltage to rise to the average value of the waveform, which by definition is $\alpha \times m_4 V_1 / 2$. Therefore, we have

$$m_4 V_1 (1 - e^{-t_{\text{dr}}/\tau_2}) \Rightarrow t_{\text{dr}} = \tau_2 \ln(2) - \tau_2 \ln(2 - \alpha). \quad (25)$$

When diode clamping occurs, i.e., $m_4 V_1 \geq V_D$ or $\beta \geq 1$, the peak value of the envelope voltage is limited to $V_D$. Therefore, its average value is given by $\alpha \times V_D / 2$. The delay is still given by the time it takes for the voltage to reach this value, so we have

$$m_4 V_1 (1 - e^{-t_{\text{dr}}/\tau_2}) \Rightarrow t_{\text{dr}} = \tau_2 \ln(2) - \tau_2 \ln \left(2 - \frac{\alpha V_D}{m_4 V_1}\right) = \tau_2 \ln(2) - \tau_2 \ln \left(2 - \frac{\alpha}{\beta}\right). \quad (26)$$

### B. Derivation of Equation (23)

We want to calculate the normalized mean, i.e., $\xi_\alpha$, of the input to each envelope detector in the external unit. For mathematical convenience, we instead calculate the normalized mean voltage envelope across the internal resonator. The two quantities are equal since they are related to each other by the transfer function.
of the external resonator, which is that of a linear lowpass filter with respect to the envelope.

The internal resonator waveform, as shown in Fig. 26, has slow rising edges but fast falling edges. Therefore, it is zero everywhere within "0" bit periods. In other words, "0" bits do not contribute to the mean value. To find the mean we therefore start by decomposing the "1" bits into runs of 1, 2, 3, . . . , n consecutive "1s" and finding $\bar{v}_2(1), \bar{v}_2(2), \ldots, \bar{v}_2(n)$, the mean value in each case. The mean value of the entire waveform, $\bar{v}_2$, can now be obtained by summing up, with appropriate probability weighting factors, $\bar{v}_2(n)$ for different values of $n$. The $n$-th term in the summation must be weighted by the product of two terms. The first is the probability that a run of $n$ "1" bits occurs, i.e., from (21), $P_{1,n} = 1/2^{n+2}$. The second term is the number of "1" bits, which is simply $n$.

For mathematical convenience, we consider very long sequences, i.e., $N \rightarrow \infty$. The exponential decrease in $P_{1,n}$ with $n$ makes the resultant infinite sum a very good approximation to the actual mean voltage even for relatively small values of $N$ (for example, our on-chip implementation used $N = 17$). Therefore, $\bar{v}_2$ is well approximated by

$$\bar{v}_2 = \sum_{n=1}^{\infty} n P_{1,n} \bar{v}_2(n) = \sum_{n=1}^{\infty} \frac{n}{2^{n+2}} \bar{v}_2(n).$$

(27)

The parameter $\alpha$ is defined as the normalized mean voltage and is therefore given by

$$\alpha = \frac{\bar{v}_2}{m_0 V_1 / 2}, \quad \beta < 1,$$

$$\alpha = \frac{\bar{v}_2}{V_D / 2}, \quad \beta \geq 1.$$  

(28)

Now we just need to find $\bar{v}_2(n)$ for two different cases: with and without diode clamping. As shown in Fig. 26(a), when diode clamping is absent, i.e., $\beta < 1$, $\bar{v}_2(n)$ is given by

$$\bar{v}_2(n) = \frac{1}{nT} \int_0^n m_d V_1 (1 - e^{-t/\tau_2}) dt$$

$$= m_d V_1 \left[ 1 - \frac{\tau_2}{nT} (1 - e^{-nT/\tau_2}) \right]$$

(29)

where $T$ is the bit period. When diode clamping is present [as shown in Fig. 26(b)], i.e., $\beta \geq 1$, the mean is given by

$$\bar{v}_2(n) = \frac{1}{nT} \int_0^{nT - t_d} m_d V_1 (1 - e^{-t/\tau_2}) dt + V_D \frac{(nT - t_d)}{nT}$$

$$= V_D \left[ 1 - \frac{t_d}{nT} (1 - \beta) - \frac{\bar{v}_2}{nT} (1 - e^{-t_d/\tau_2}) \right]$$

(30)

where $t_d$ is the time taken by the envelope to reach the clamp voltage $V_D$. Its value can be calculated using

$$m_d V_1 (1 - e^{-t_d/\tau_2}) = V_D.$$  

(31)

Substituting (31) in (30) and simplifying, we get

$$\bar{v}_2(n) = V_D \left[ 1 - \frac{\tau_2}{nT} (1 + (1 - \beta)(1 - 1/\beta)) \right].$$

(32)

Evaluating the sum in (27) for both cases ($\beta < 1$ and $\beta \geq 1$, respectively) and using the definition of $\alpha$ as given by (28) gives us (23).

C. Radiated Emissions

Regulatory issues are a concern for any implanted medical devices. Unfortunately, none of the unlicensed ISM frequency bands below 433 MHz have enough bandwidth to support uplink data rates larger than a few hundred kbits/sec (the widest band, centered around 27.12 MHz, is only 670 KHz wide). Therefore, high-data-rate systems like our uplink cannot hope to fit within an ISM band. Permissible radiation limits in the United States for unlicensed, low-power wireless devices operating outside ISM bands are set forth in Part 15 of the F.C.C. rules (Title 47 of the Code of Federal Regulations). According to the code, radiated emissions between 1.705 and 30.0 MHz (with the exception of certain restricted frequency bands) must not exceed $30 \mu V/m$ at a distance of 30 m from the device.

We now perform a simple analysis to see whether F.C.C. regulations on radiated emissions are likely to be a concern for our system. A formula that predicts the radiation resistance $R_{rad}$ of a small (much smaller than the wavelength $\lambda$) circular loop of $N$ turns is (see, for example, [33])

$$R_{rad} \approx 3.1171 \times 10^{4} N^2 \left( \frac{S^2}{\lambda^4} \right) \Omega$$

(33)

where $S$ is the area of the coil. Approximating our square external coil, which is 3.5 cm on a side and has $N = 2$ turns, as a circular coil with the same area and number of turns, we get $R_{rad} = 0.013 \Omega$ for $\lambda = 12$ m (25 MHz). The radiated power is given by $P_{rad} = I^2 R_{rad}$, where $I$ is the amplitude of the AC current in the coil. With $I = 1$ mA, a typical value for our design, we get $P_{rad} = 13$ nW. The maximum radiated power density ($W/m^2$) at a distance $R$ from the coil is

$$P_{learn} = \frac{D_0 P_{rad}}{4\pi R^2}$$

(34)

where $D_0 = 1.5$ is the maximum gain produced by a small loop antenna. We also have $P_{learn} = E_{rad}^2 / Z_0$, where $E_{rad}$ is the radiated electric field and $Z_0 = 120 \pi \Omega$ is the impedance of free space. Plugging numbers into (34) for $R = 30$ m gives us $E_{rad} = 25.5 \mu V/m$, which just meets the F.C.C. specification. Going to higher center frequencies with the current coil design is inadvisable since $\lambda$ would decrease, increasing $R_{rad}$. Similarly, using a bigger coil, or one with more turns, would also cause $R_{rad}$ to increase.

ACKNOWLEDGMENT

The authors wish to thank S. K. Arfin for help with figures and photography, and the anonymous reviewers.

REFERENCES


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